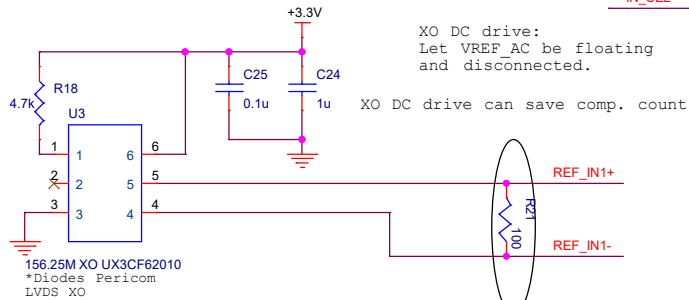
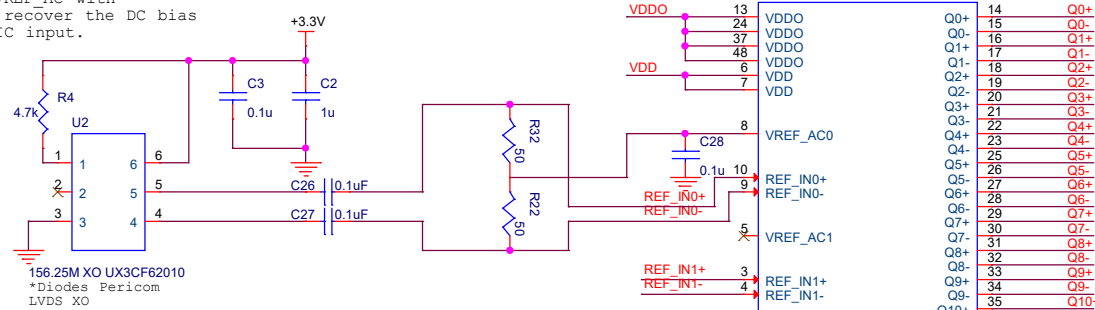


XO AC drive:
Connect VREF_AC with
0.1uF to recover the DC bias
for the IC input.



Closed to IC<200 mil

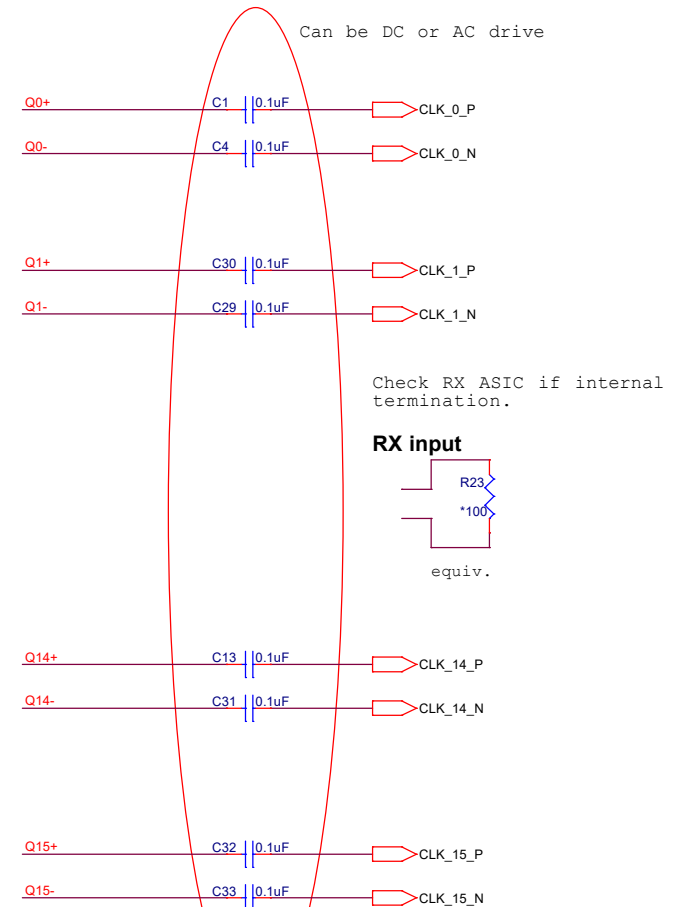
Device setting:

Input IN_SEL:

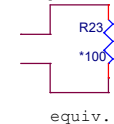
0: REF_IN0 is reference input
1: REF_IN1 is reference input
Open: No inputs selected. Output Hi-Z

App Note:

1. Select REF_IN0 or REF_IN1 as input ;
- 2.1 Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD, VDDO...etc)
- 2.2 VDD use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. Suggest to use DC coupling in LVDS drive input clock with 100ohm corss at input pins <200mil;
4. when in AC input drive VREF_AC is used.
5. Q0 to Q15 are LVDS output (1.2V+/- 200mV), can do DC to LVDS drive, or AC to drive other diff. input
6. If use CMOS XO drive, needs 1k pull-up/down at REF_IN- pin, refer to datasheet app. page
7. Connect EPAD in >=12 vias to GND plane



RX input



Title		
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